WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

a semiconductor chip having a memory cell array region and a peripheral circuit region surrounding the memory cell array region; and

a plurality of bonding pads disposed on only one side of the semiconductor chip on the peripheral circuit region.

2. The device of claim 1, wherein the plurality of bonding pads are disposed in at least one row.

3. The device of claim 2, wherein the plurality of bonding pads are disposed in two rows.

4. The device of claim 3, further comprising:

a plurality of leads formed over a portion of the semiconductor chip.

5. The device of claim 4, further comprising:

a plurality of bonding wires electrically connecting the plurality of leads, respectively, with a portion of the bonding pads.

6. The device of claim 2, further comprising:

a plurality of leads formed over a portion of the semiconductor chip.

7. The device of claim 6, further comprising:

a plurality of bonding wires electrically connecting the plurality of leads, respectively, with a portion of the bonding pads.

8. The device of claim 2, further comprising:

a first leads group disposed adjacent to the bonding pad side of the semiconductor chip;

a second leads group disposed opposite the first leads group; and

a plurality of bonding wires having a first plurality of bonding wires and a second plurality of bonding wires electrically connecting the first leads group and the second leads group, respectively, with the plurality of bonding pads.

9. The device of claim 8, wherein the second leads group disposed opposite the first leads group are located to a side of the semiconductor chip opposite the bonding pad side.

10. The device of claim 8, wherein the plurality of bonding pads are electrically connected alternately with the first leads group and the second leads group by the

first plurality of bonding wires and the second plurality of bonding wires, respectively, the first plurality of bonding wires being disposed over the peripheral circuit region, the second plurality of bonding wires being disposed over the memory cell array region.

11. The device of claim 8, wherein the plurality of bonding pads are disposed in a first row and a second row, the first row of bonding pads and the second row of bonding pads being electrically connected to the first leads group and the second leads group, respectively, by the first plurality of bonding wires and the second plurality of bonding wires, the first plurality of bonding wires being disposed over the peripheral circuit region, and the second plurality of bonding wires being disposed over the memory cell array region.

12. The device of claim 8, wherein the second leads group extends over a portion of the semiconductor chip region.

13. The device of claim 12, wherein the plurality of bonding pads are electrically connected alternately with the first leads group and the second leads group by the first plurality of bonding wires and the second plurality of bonding wires, respectively, the first plurality of bonding wires being disposed over the peripheral circuit

region, the second plurality of bonding wires being disposed over the memory cell array region.

14. The device of claim 12, wherein the plurality of bonding pads are disposed in a first row and a second row, the first row of bonding pads and a second row of bonding pads being electrically connected to the first leads group and the second leads group, respectively, by the first plurality of bonding wires and the second plurality of bonding wires, the first plurality of bonding wires being disposed over the peripheral circuit region, and the second plurality of bonding wires being disposed over the memory cell array region.